REMARKS

Claims 1-6 are all the claims pending in the application. Claims 1, 2, 3 and 6 have been amended.

Claim Objections/Minor Informalities

Claim 3 is objected to because there is no antecedent basis for "said variable delay clock". The Examiner suggests that the word "said" be changed to --a--. This change has been made, as seen in the amended claims.

Claim Rejections - 35 U.S.C. § 102

Claims 1-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al (6,326,826). This rejection is traversed for at least the following reasons.

Lee et al

In comparing the claimed invention to the teachings in the newly cited patent to Lee et al, the Examiner asserts that Lee et al teaches all of the features of the claimed invention. Figure 1 of the reference illustrates a delay locked loop circuit where a reference clock REF_CK is provided to a phase detector 13, that also receives a phase controlled clock output CK[1:7] from a delay chain 11 and provides control inputs PUP, PDOWN to a first charge pump 15. The reference clock and phase controlled clock are also provided to a frequency detection logic 12, having an output to a second charge pump 14. The two charge pumps provide an input to a common terminal of a loop filter 16, whose output is provided as a delay control to the delay elements of the delay chain 11. Details of a representative delay cell are provided in Fig. 1 and details of the charge pumps are provided in Fig. 5.

While the circuit on its face may appear to resemble the circuit in Fig. 1 of the present application, there is a significant and notable distinction. Specifically, in Lee et al, the first charge pump 15 is used for removing remaining phase error. The first charge pump 15 is not relevant to an operation of the loop during realization of locking of frequency, as explained at column 2, lines 63 to 65 of the patent. Moreover, the first charge pump 15 is used for removing remaining phase error, and it is not used for effecting the spread of spectrum by modulating the clock. As explained at col. 3, lines 1-5, once frequency lock is achieved and the charge pump 15 is engaged, the phased detector and charge pump finely tune out the remaining phase error between the reference clock and the clock CK[7]. It does not continually contribute to spread spectrum, as in the present invention.

This distinction is supported by several additional differences. A first difference is the use of a frequency detection logic 12, which serves as an input to the charge pump 14. The purpose of this structure is to provide a frequency adjustment capability, which was lacking in the conventional art, as described at col. 1, lines 52-59. Moreover, as explained at col. 2, line 59-col. 3, line 5, the operation of the phase detector 13 and the frequency detection logic 12 are alternatively provided, such that the charge pump 14 charges or discharges the filter in response to the detected frequency, while the phase detector 13 and charge pump 15 are disabled. Once frequency lock is obtained, the phase detector 13 operates and the frequency detector is disabled, thereby allowing the charge pump 15 to be operational to finely tune the remaining phase error between the reference clock and the output clock.

A second difference is that the present invention has the capacity of the second pump larger than the first, as explained at page 10, first full paragraph. of the specification. This feature has been added by amendment to claim 2 and already is recited in claim 6.

A third difference, with respect to all of the claims, is the express goal of the present invention to spread a spectrum of the phase controlled clock outputted at the output of the circuit. As explained at pages 9-17 of the application, the variable delay circuit 2 of the DLL circuit 10 is controlled to spread the spectrum of the of the output clock Mclk. Details of this process are disclosed with respect to Fig. 5. In particular, the present application teaches a unique manner in which the operational state of the variable delay circuit 2, namely, the phase difference of the modulated clock to the reference clock created by the delay is detected, and the way the delay setting circuit 11 varies the setting for generating the input control voltage to the variable delay circuit that generates the spectrum spread modulation clock according to the detected result of the phase difference. In particular, as stated at pages 16-17, the delay setting circuit 11 instructs the second charge pump 12 to take out the charge DQ corresponding to Dt, so as to give the control voltage DV required for delaying the phase and changing the clock cycle by Dt to the variable delay circuit 2 as the control input.

Notably, there is no mention in Lee et al of a manner of achieving a spread spectrum effect or even a desire to achieve a spread spectrum effect. The focus of the disclosure in Lee et al is on accommodating a wide frequency range and removing phase error. The Examiner cannot assert that any modulation of the reference clock signal will accomplish some measure of spread spectrum because, as already noted, Lee is focused only on removing remaining phase error and not for effecting the spread spectrum by modulating the clock, as previously noted with regard to the disclosure at col. 2, lines 63-65. This is not be relevant to spread spectrum.

Finally, with respect to the limitations in the dependent claims 3-5, the Examiner merely asserts that the limitations are taught in or inherent in the structure of Lee et al. However, Applicants respectfully submit that the Examiner has not demonstrated how and why these limitations are actually met on the basis of the disclosure of Lee et al. In the absence of a specific teaching of these limitations, the claims cannot be anticipated or rendered obvious.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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